WHAT IS CLAIMED IS:

1. A semiconductor device having a metal oxide semiconductor (MOS) type transistor structure, comprising:

an additional load capacitance that is formed at a part of the semiconductor device, which is vulnerable to soft errors.

2. The semiconductor device according to claim 1, wherein the part that is vulnerable to soft errors is a first diffusion layer region, and the first diffusion layer region is at least a part of diffusion layer regions formed in the MOS type transistor structure and is connected to neither a power supply nor a ground.

3. The semiconductor device according to claim 1, wherein the formation of the additional load capacitance is performed such that a well region that is formed immediately below the first diffusion layer region is made to have a higher concentration than other well region.

4. The semiconductor device according to claim 3, wherein an impurity concentration at a junction interface between the well region with the higher concentration and the first diffusion layer region is set at 5×10^{18} to $10^{19}/cm^3$, and an impurity concentration at a junction interface between the other well region and a second diffusion layer region which is the diffusion layer regions except for

the first diffusion layer region is set at $10^{18}/cm^3$.

5. The semiconductor device according to claim 1, wherein the semiconductor device having the MOS type transistor structure includes at least an n-type MOS transistor, and

the part that is vulnerable to soft errors is a drain of the n-type MOS type transistor.

6. The semiconductor device according to claim 5, wherein the semiconductor device having the MOS type transistor structure is a static random access memory (SRAM) type memory cell having a flip-flop circuit that comprises a plurality of the n-type MOS transistors and a plurality of p-type MOS transistors.

7. The semiconductor device according to claim 1, wherein the semiconductor device having the MOS type transistor structure includes at least an n-type MOS transistor and a p-type MOS transistor, and

the part that is vulnerable to soft errors is a drain of the n-type MOS transistor and a drain of the p-type MOS transistor.

8. The semiconductor device according to claim 7, wherein the semiconductor device having the MOS type transistor structure is a static random access memory (SRAM) type memory cell having a flip-flop circuit that comprises a plurality of the n-type MOS transistors and a plurality of the p-type MOS transistors.

9. A semiconductor device having a metal oxide

semiconductor (MOS) type transistor structure, comprising:

a buried well region that is formed at a part of the semiconductor device, which is vulnerable to soft errors.

10. The semiconductor device according to claim 9, wherein the part that is vulnerable to soft errors is a first diffusion layer region, and the first diffusion layer region is at least a part of diffusion layer regions formed in the MOS type transistor structure and is connected to neither a power supply nor a ground.

11. The semiconductor device according to claim 9, wherein the formation of the buried well region is performed such that a well region that is formed immediately below the first diffusion layer region is made to have a triple-well structure.

12. The semiconductor device according to claim 11, wherein the well region that is formed immediately below the first diffusion layer region, where the buried well region is formed, is made to have a triple-well structure, and other well region is made to have a twin-well structure.

13. The semiconductor device according to claim 9, wherein the semiconductor device having the MOS type transistor structure includes at least an n-type MOS transistor, and

the part that is vulnerable to soft errors is

a drain of the n-type MOS type transistor.

14. The semiconductor device according to claim 13, wherein the semiconductor device having the MOS type transistor structure is a static random access memory (SRAM) type memory cell having a flip-flop circuit that comprises a plurality of the n-type MOS transistors and a plurality of p-type MOS transistors.

15. The semiconductor device according to claim 9, wherein the semiconductor device having the MOS type transistor structure includes at least an n-type MOS transistor and a p-type MOS transistor, and

the part that is vulnerable to soft errors is a drain of the n-type MOS transistor and a drain of the p-type MOS transistor.

16. The semiconductor device according to claim 15, wherein the semiconductor device having the MOS type transistor structure is a static random access memory (SRAM) type memory cell having a flip-flop circuit that comprises a plurality of said n-type MOS transistors and a plurality of said p-type MOS transistors.

17. A method of manufacturing a semiconductor device having a metal oxide semiconductor (MOS) type transistor structure, comprising:

specifying by circuit simulation a part of the semiconductor device, which is vulnerable to soft errors; and

forming an additional load capacitance at the part of the semiconductor device, which is vulnerable to soft errors.

18. The method of manufacturing a semiconductor device, according to claim 17, wherein the formation of the additional load capacitance is performed such that additional ion implantation is selectively performed in addition to ordinary ion implantation at a time of forming a well region in the MOS type transistor structure, whereby a well region having a higher concentration than the other well region is formed at the part that is vulnerable to soft errors.

19. A method of manufacturing a semiconductor device having a metal oxide semiconductor (MOS) type transistor structure, comprising:

specifying by circuit simulation a part of the semiconductor device, which is vulnerable to soft errors; and

forming a buried well region at the part of the semiconductor device, which is vulnerable to soft errors.

20. The method of manufacturing a semiconductor device, according to claim 19, wherein the formation of the buried well region is performed such that the well region of the part that is vulnerable to soft errors is made to have a triple-well structure, and the other well region is made to have a twin-well structure.